PATENT
Attorney Docket No. 401263/FUKAMI

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

ABE et al.

Art Unit: Unknown

Application No.: Unknown

Examiner: Unknown

Filed: June 28, 2001

For: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Prior to the examination of the above-identified patent application, please enter the following amendments and consider the following remarks.

IN THE DRAWINGS:

The Examiner is requested to approve the changes to Figures 9-21 and 29-35 as indicated in the attached Request for Approval of Drawing Amendments.

IN THE SPECIFICATION:

Replace the paragraph beginning at page 2, line 1 with:

Through never-ending progress in downsizing of semiconductor chips, a semiconductor chip is now almost thinner than a lead frame. Such semiconductor chips have become highly dense, while densification of a semiconductor device mounting these semiconductor chips is insufficient. In particular, current semiconductor devices are not thin enough as thinning thereof has rarely received attention. Then, with a rapid

prevalence of mobile data terminals like mobile phones, digital cameras, video camera and the like, there arise strong demands for downsizing and densification in consideration of the thickness of a semiconductor device. Downsizing and densification of a semiconductor device with its thickness reduced without an increase in area would provide desirable effects not only in such uses as mentioned above but in many other uses.

Replace the paragraph beginning at page 11, line 10 with:

Figs. 10, 11, 12, and 13 respectively show cross sections along lines X-X, XI-XI, XII-XII, and XIII-XIII in Fig. 9.

Replace the paragraph beginning at page 11, line 12 with:

Figs. 14, 15, 16, and 17 respectively show cross sections of a semiconductor device according to a first modification of the first embodiment of the present invention corresponding to respective cross sections along lines X-X, XI-XI, XII-XII, and XIII-XIII in Fig. 9.

Replace the paragraph beginning at page 11, line 16 with:

Figs. 18, 19, 20, and 21 respectively show cross sections of a semiconductor device according to a second modification of the first embodiment of the present invention corresponding to respective cross sections along lines X-X, XI-XI, XII-XII, and XIII-XIII in Fig. 9.

Replace the paragraph beginning at page 12, line 4 with:

Figs. 30 31, 32, and 33 respectively show cross sections along lines XXX-XXX, XXXI-XXXI, XXXII-XXXII, and XXXIII-XXXIII in Fig. 29.

Replace the paragraph beginning at page 12, line 6 with:

Fig. 35 shows a cross section along line XXXV-XXXV in Fig. 34.

Replace the paragraph beginning at page 14, line 14 with:

Figs. 10, 11, 12, and 13 show respective cross sections along lines X-X, XI-XI, XII-XII, and XIII-XIII in Fig. 9. Components that are exposed after the adhesive tape is removed are encapsulated and fastened by means of an encapsulating resin. Although Figs. 10 to 13 show no wire connecting semiconductor chips 1a and 1b with leads 4a, the encapsulating resin has a thickness sufficient to encapsulate wires.

Replace the paragraph beginning at page 14, line 25 with:

A first modification of the first embodiment according to the present invention is described below. Figs. 14, 15, 16, and 17 respectively show cross sections of a semiconductor device corresponding to those along respective lines X-X, XI-XI, XII-XII, and XIII-XIII in Fig 9. In the first modification, a die pad 4b is processed such that it is shifted upward slightly. Naturally, according to the upward shifting of the die pad, upper and lower semiconductor chips 1a and 1b are both shifted upward. Other components are identical in structure to those of the first embodiment. An encapsulating resin thus extends under lower semiconductor chip 1b. Therefore, when an adhesive sheet is removed, lower semiconductor chip 1b and die pad 4b are never exposed on the rear side.

Replace the paragraph beginning at page 15, line 17 with:

Figs. 18, 19, 20 and 21 respectively show cross sections of a semiconductor device according to a second modification of the first embodiment, corresponding to those along respective lines X-X, XI-XI, XII-XII, and XIII-XIII in Fig 9. The second modification is characterized by the difference in thickness between upper and lower semiconductor chips 1a and 1b as compared with the embodiment discussed above. Other components are identical in structure to those of the first modification. A die pad 4b of the second modification is also shifted upward and thus the manufacturing method of the first modification can be applied.

Replace the paragraph beginning at page 17, line 16 with:

Figs. 30, 31, 32, and 33 are cross sections respectively along lines XXX-XXX, XXXI-XXXI, XXXII-XXXII, and XXXIII-XXXIII in Fig. 29. It can be understood from

these drawings that the thickness of a semiconductor device of TSOP type can be reduced by arranging two semiconductor chips in the region surrounded by lead frames. In addition, the manufacturing method of the second embodiment employing spot welding to accomplish efficient production is suitable for low cost and mass production of semiconductor devices.

IN THE CLAIMS:

Replace the indicated claims with:

1. (Amended) A semiconductor device having:

terminal electrodes located, in plan view, outside a region where semiconductor chips are located;

a lower semiconductor chip overlapping in height with said terminal electrodes;

an upper semiconductor chip located opposite said lower semiconductor chip;

wires connecting said upper and lower semiconductor chips to said terminal electrodes; and

an encapsulating resin encapsulating said upper and lower semiconductor chips and said wires, wherein said encapsulating resin and said terminal electrodes have respective bottom surfaces coplanar with each other.

2. (Amended) The semiconductor device according to claim 1, including a die pad supporting said upper semiconductor chip and coplanar with said terminal electrodes, and wherein said lower semiconductor chip does not overlap, in plan view, said die pad.

3. (Amended) The semiconductor device according to claim 1, wherein said lower semiconductor chip and said encapsulating resin have respective bottom surfaces coplanar with each other and the bottom surface of said lower semiconductor chip is exposed and not covered by said encapsulating resin.

4. (Amended) The semiconductor device according to claim 1, including a die pad supporting said upper semiconductor chip and not coplanar with said terminal

electrodes, and wherein said lower semiconductor chip has a bottom surface encapsulated by said encapsulating resin.

5. (Amended) The semiconductor device according to claim 1, wherein said semiconductor device is a QFN (Quad Flat Non-Lead) Package having said terminal electrodes surrounding said upper and lower semiconductor chips.

6. (Amended) The semiconductor device according to claim 1, wherein said upper and lower semiconductor chips are respectively rectangular in shape, connection terminals of said upper and lower semiconductor chips are arranged along shorter sides of said upper and lower semiconductor chips, opposing each other, and said upper and lower semiconductor chips cross each other, in plan view.

7. (Amended) The semiconductor device according to claim 1, wherein said terminal electrodes are leads located along two opposing sides of said semiconductor device with said upper and lower semiconductor chips therebetween.

8. (Amended) A semiconductor device TSOP (Thin Small Outline) Package having:

upper and lower semiconductor chips arranged between a first lead portion and a second lead portion, respectively, on two opposing sides of said semiconductor device, in plan view;

a first die pad integrated with and not coplanar with said first lead portion and located on one side of a reference plane passing through a central position between a first surface and a second surface of said first and second lead portions; and

a second die pad integrated with and not coplanar with said second lead portion and located on a second side of the reference plane, wherein said lower semiconductor chip is supported by said first die pad and said upper semiconductor chip is supported by said second die pad portion, said upper and lower semiconductor chips are partially overlapping and overlap in height with said first and second lead portions.

9. (Amended) The semiconductor device according to claim 8, including:

a first lead frame connected to said first die pad and located, with said first lead portion, on the first side of said reference plane, and

a second lead frame connected to said first die pad and located, with said second lead portion, on the second side of said reference plane.

10. (Amended) The semiconductor device according to claim 9, wherein

said first die pad portion is L-shaped and includes a first extension extending from an end of said first lead portion toward said second lead portion, and a first opposing portion continuing from said first extension and extending parallel to said first lead portion,

said second die pad portion is arranged, in plan view, opposite said first die pad , is L-shaped, and includes a second extension extending from an end of said second lead portion toward said first lead portion and a second opposing portion continuing from said second extension and extending parallel to said second lead portion,

said first extension and said first opposing portion have bottom surfaces supporting said lower semiconductor chip, and

said second extension and said second opposing portion have upper surfaces supporting said upper semiconductor chip.

11. (Amended) The semiconductor device according to claim 8, wherein said first and second lead portions and said first and second die pads are integrated into a common lead frame, said reference plane passes centrally through the thickness of said lead frame, said first die pad supports said lower semiconductor chip of said partially overlapped upper and lower semiconductor chips, and said second die pad supports said upper semiconductor chip.

12. (Amended) The semiconductor device according to claim 11, including adhesive layers respectively bonding said upper and lower semiconductor chips to said first and second die pads wherein a center of the thickness of said first die pad portion and a center of the thickness of said second die pad portion are spaced from said reference

plane in respective opposite directions, each by a distance equal to the sum of one-half the thickness of said lead frame and one-half the thickness of said adhesive layers bonding said upper and lower semiconductor chips to said first and second die pads.

13. (Amended) A method of manufacturing a semiconductor device comprising:

stacking a first lead frame on a second lead frame, said first lead frame including a first lead portion and a first die pad extending in an L-shape from an end of said first lead portion along a periphery of a region where a lower semiconductor chip is arranged, said second lead frame including a second lead portion and a second die pad opposing said first die pad, in plan view, and extending in an L-shape from an end of said second lead portion along a periphery of a region where an upper semiconductor chip is arranged, said first and second lead portions being opposite each other, in plan view, with said upper and lower semiconductor chips therebetween;

bonding said lower semiconductor chip to said first die pad and bonding said upper semiconductor chip to said second die pad;

welding together said first lead frame and said second lead frame where they overlap;

connecting said upper and lower semiconductor chips to a terminal electrode with a wire;

encapsulating in a resin a region inside of said first and second lead frames that have been welded; and

cutting off a portion, outside said resin, encapsulating said first and second lead portions and said upper and lower semiconductor chips.

14. (Amended) The method of manufacturing a semiconductor device according to claim 13, including combining stacking of said first and second lead frames and bonding of said upper and lower semiconductor chips, and wherein sub steps in the lead frame stacking and sub steps in the semiconductor chip bonding are partially changed in their order.

bonding of said upper and lower semiconductor chips, and wherein bonding said upper and lower semiconductor chips includes arranging a die bonding material for bonding said upper and lower semiconductor chips to said first and second die pad.

IN THE ABSTRACT:

Replace the Abstract with:

ABSTRACT OF THE DISCLOSURE

A semiconductor device and a manufacturing method for downsizing and densification achieved by reducing the thickness of the semiconductor device without an increase in area. Terminal electrodes are arranged, in plan view, outside a region where semiconductor chips are arranged. A lower semiconductor chip is placed overlapping in height the terminal electrodes, an upper semiconductor chip is placed above the lower semiconductor chip, wires connect the upper and lower semiconductor chips to the terminal electrodes, and an encapsulating resin encapsulates the upper and lower semiconductor chips and wires. The encapsulating resin has its bottom surface coplanar with the bottom surface of the terminal electrodes.

REMARKS

The foregoing Amendment corrects translational errors and conforms the claims to United States practice.

Respectfully submitted,

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SPECIFICATION, CLAIMS AND ABSTRACT AS PRELIMINARILY AMENDED

Amendments to the paragraph beginning at page 2, line 1:

Through never-ending progress in downsizing of semiconductor chips, a semiconductor chip is now almost thinner than a lead frame. Such semiconductor chips have become highly dense, while densification of a semiconductor device mounting these semiconductor chips is insufficient. In particular, current semiconductor devices are not thin enough as thinning thereof has rarely received attention. Then, with a rapid prevalence of mobile data terminals like mobile ~~phone~~ phones, digital ~~camera~~ cameras, video camera and the like, there arise strong demands for downsizing and densification in consideration of the thickness of a semiconductor device. Downsizing and densification of a semiconductor device with its thickness reduced without an increase in area would provide desirable effects not only ~~to~~ in such uses as mentioned above but ~~to~~ in many other uses.

Amendments to the paragraph beginning at page 11, line 10:

Figs. 10 ~~to~~, 11, 12, and 13 respectively show cross sections along ~~A-A', B-B', C-C' and D-D'~~ lines X-X, XI-XI, XII-XII, and XIII-XIII in Fig. 9.

Amendments to the paragraph beginning at page 11, line 12:

Figs. 14~~-to~~, 15, 16, and 17 respectively show cross sections of a semiconductor device according to a first modification of the first embodiment of the present invention corresponding to respective cross sections along~~-A-A', B-B', C-C' and D-D'~~ lines X-X, XI-XI, XII-XII, and XIII-XIII in Fig. 9.

Amendments to the paragraph beginning at page 11, line 16:

Figs. 18~~-to~~, 19, 20, and 21 respectively show cross sections of a semiconductor device according to a second modification of the first embodiment of the present invention corresponding to respective cross sections along~~-A-A', B-B', C-C' and D-D'~~ lines X-X, XI-XI, XII-XII, and XIII-XIII in Fig. 9.

Amendments to the paragraph beginning at page 12, line 4:

Figs. 30~~-to~~ 31, 32, and 33 respectively show cross sections along~~-A-A', B-B', C-C' and D-D'~~ lines XXX-XXX, XXXI-XXXI, XXXII-XXXII, and XXXIII-XXXIII in Fig. 29.

Amendments to the paragraph beginning at page 12, line 6:

Fig. 35 shows a cross section along~~-A-A'~~ line XXXV-XXXV in Fig. 34.

Amendments to the paragraph beginning at page 14, line 14:

Figs. 10~~-to~~, 11, 12, and 13 show respective cross sections along~~-A-A', B-B', C-C' and D-D'~~ lines X-X, XI-XI, XII-XII, and XIII-XIII in Fig. 9. Components that are exposed after the adhesive tape is removed are encapsulated and fastened by means of an encapsulating resin. Although Figs. 10 to 13 show no wire connecting semiconductor chips 1a and 1b with leads 4a, the encapsulating resin has a thickness sufficient to encapsulate wires.

Amendments to the paragraph beginning at page 14, line 25:

A first modification of the first embodiment according to the present invention is described below. Figs. 14~~-to~~, 15, 16, and 17 respectively show cross sections of a

semiconductor device corresponding to those along respective lines ~~A-A', B-B', C-C' and D-D'~~ X-X, XI-XI, XII-XII, and XIII-XIII in Fig 9. In the first modification, a die pad 4b is processed such that it is shifted upward slightly. Naturally, according to the upward shifting of the die pad, upper and lower semiconductor chips 1a and 1b are both shifted upward. Other components are identical in structure to those of the first embodiment. An encapsulating resin thus extends under lower semiconductor chip 1b. Therefore, when an adhesive sheet is removed, lower semiconductor chip 1b and die pad 4b are never exposed on the rear side.

Amendments to the paragraph beginning at page 15, line 17:

Figs. 18~~to~~, 19, 20 and 21 respectively show cross sections of a semiconductor device according to a second modification of the first embodiment, corresponding to those along respective lines ~~A-A', B-B', C-C' and D-D'~~ X-X, XI-XI, XII-XII, and XIII-XIII in Fig 9. The second modification is characterized by the difference in thickness between upper and lower semiconductor chips 1a and 1b as compared with the embodiment discussed above. Other components are identical in structure to those of the first modification. A die pad 4b of the second modification is also shifted upward and thus the manufacturing method of the first modification can be applied.

Amendments to the paragraph beginning at page 17, line 16:

Figs. 30~~to~~, 31, 32, and 33 are cross sections respectively along ~~A-A', B-B', C-C' and D-D'~~ lines XXX-XXX, XXXI-XXXI, XXXII-XXXII, and XXXIII-XXXIII in Fig. 29. It can be understood from these drawings that the thickness of a semiconductor device of TSOP type can be reduced by arranging two semiconductor chips in the region surrounded by lead frames. In addition, the manufacturing method of the second embodiment employing spot welding to accomplish efficient production is suitable for low cost and mass production of semiconductor devices.

Amendments to existing claims:

1. (Amended) A semiconductor device having:

terminal electrodes ~~arranged~~ located, in plan view, outside a region where semiconductor chips are ~~arranged, comprising:~~ located;

a lower semiconductor chip ~~located to overlap~~ overlapping in ~~the range of~~ height with said terminal electrodes;

an upper semiconductor chip located ~~above~~ opposite said lower semiconductor chip;

~~a wire~~wires connecting said upper and lower semiconductor chips to said terminal electrodes; and

an encapsulating resin encapsulating said upper and lower semiconductor chips and said ~~wire~~ wires, wherein said encapsulating resin and said terminal electrodes ~~having~~ have respective bottom surfaces coplanar with each other.

2. (Amended) The semiconductor device according to claim 1, ~~wherein~~ including a die pad supporting said upper semiconductor chip ~~is supported by a die pad portion~~ and coplanar with said terminal electrodes, and wherein said lower semiconductor chip ~~is arranged without overlapping~~ does not overlap, in plan view, ~~with~~ said die pad ~~portion~~.

3. (Amended) The semiconductor device according to claim 1, wherein said lower semiconductor chip and said encapsulating resin have respective bottom surfaces coplanar with each other and the bottom surface of said lower semiconductor chip is exposed ~~from~~ and not covered by said encapsulating resin.

4. (Amended) The semiconductor device according to claim 1, ~~wherein~~ including a die pad supporting said upper semiconductor chip ~~is supported by a die pad portion located higher than~~ and not coplanar with said terminal electrodes, and wherein said lower semiconductor chip has ~~its~~ a bottom surface encapsulated by said encapsulating resin.

5. (Amended) The semiconductor device according to claim 1, wherein said semiconductor device is ~~of~~ a QFN (Quad Flat Non-Lead) Package ~~type~~ having said terminal electrodes ~~arranged outside to surround~~ surrounding said upper and lower semiconductor chips.

6. (Amended) The semiconductor device according to claim 1, wherein said upper and lower semiconductor chips are ~~rectangles~~ respectively rectangular in shape, connection terminals of ~~the~~ said upper and lower semiconductor chips are arranged along shorter sides of said upper and lower semiconductor chips, opposing each other ~~of said rectangles~~, and said upper and lower semiconductor chips ~~being rectangles in shape are arranged to~~ cross each other, in plan view.

7. (Amended) The semiconductor device according to claim 1, wherein said terminal electrodes ~~arranged outside~~ are leads ~~arranged~~ located along two opposing sides of said semiconductor device with said upper and lower semiconductor chips therebetween.

8. (Amended) A semiconductor device ~~of~~ TSOP (Thin Small Outline) Package ~~type~~ having:

upper and lower semiconductor chips arranged between a first lead portion and a second lead portion ~~provided~~, respectively, on two ~~sides~~ opposing sides of said semiconductor device, in plan view ~~, comprising:~~;

a first die pad ~~portion~~ integrated with and ~~noncoplanar~~ not coplanar with said first lead portion and located ~~higher relative to~~ on one side of a reference plane passing through a central position between ~~the highest~~ a first surface and ~~the lowest~~ a second surface of said first and second lead portions; and

a second die pad ~~portion~~ integrated with and ~~noncoplanar~~ not coplanar with said second lead portion and located ~~lower relative to said~~ on a second side of the reference plane ~~; and a~~, wherein said lower semiconductor chip is supported by said first die pad ~~portion~~ and ~~an~~ said upper semiconductor chip is supported by said second die pad portion,

said ~~two~~ upper and lower semiconductor chips ~~being~~ are partially ~~overlapped~~ overlapping and ~~located to~~ overlap in ~~the range of~~ height with said first and second lead portions.

9. (Amended) The semiconductor device according to claim 8, ~~wherein said first die pad portion is provided to~~ including:

a first lead frame connected to said first die pad and located ~~including~~, with said first lead portion ~~above~~, on the first side of said reference plane, and

~~said second die pad portion is provided to~~ a second lead frame connected to said first die pad and located ~~including~~, with said second lead portion ~~below~~, on the second side of said reference plane.

10. (Amended) The semiconductor device according to claim 9, wherein

said first die pad portion is L-shaped ~~including~~ and includes a first extension extending from an end of said first lead portion toward said second lead portion, and a first opposing portion continuing from said first extension and extending ~~in~~ parallel ~~with~~ to said first lead portion,

said second die pad portion is arranged, in plan view, opposite said first die pad ~~portion and~~, is L-shaped ~~including~~, and includes a second extension extending from an end of said second lead portion toward said first lead portion and a second opposing portion continuing from said second extension and extending ~~in~~ parallel ~~with~~ to said second lead portion,

said first extension and said first opposing portion have ~~their~~ bottom ~~surface~~ surfaces supporting said lower semiconductor chip, and

said second extension and said second opposing portion have ~~their~~ upper ~~surface~~ surfaces supporting said upper semiconductor chip.

11. (Amended) The semiconductor device according to claim 8, wherein said first and second lead portions and said first and second die ~~pad portions~~ pads are integrated into a common lead frame, said reference plane passes centrally through ~~center of~~ the thickness of said lead frame, said first die pad ~~portion~~ supports said lower

~~a resin encapsulating step of~~ encapsulating ~~by means of~~ in a resin a region inside ~~said overlapping portion being~~ of said first and second lead frames that have been welded; and

~~a cutting off step of~~ cutting off a portion, outside said resin ~~encapsulated~~, encapsulating said first and second lead ~~portion~~ portions and said upper and lower semiconductor chips ~~in said resin encapsulating step~~.

14. (Amended) The method of manufacturing a semiconductor device according to claim 13, ~~wherein~~ including combining stacking of said first and second lead ~~frame stacking step~~ frames and bonding of said upper and lower semiconductor ~~chip bonding step are combined~~ chips, and wherein sub steps ~~of said~~ in the lead frame stacking ~~step~~ and sub steps ~~of said~~ in the semiconductor chip bonding ~~step~~ are partially changed in their order ~~to be performed~~.

15. (Amended) The method of manufacturing a semiconductor device according to claim 13, ~~wherein~~ including combining stacking of said first and second lead ~~frame stacking step~~ frames and bonding of said upper and lower semiconductor ~~chip bonding step are combined~~ chips, and ~~said lead frame stacking step and said~~ wherein bonding said upper and lower semiconductor ~~chip bonding step include a die bonding material~~ chips includes arranging ~~step of arranging~~ a die bonding material for bonding said upper and lower semiconductor chips to said first and second die pad ~~portions~~.

Amendments to the abstract:

ABSTRACT OF THE DISCLOSURE

A semiconductor device and a manufacturing method ~~thereof are provided with~~ for downsizing and densification achieved by reducing the thickness of the semiconductor device without an increase in area. Terminal electrodes are arranged, in plan view, outside a region where semiconductor chips are arranged. A lower semiconductor chip is placed ~~to overlap~~ overlapping in ~~the range of~~ height ~~with~~ the terminal electrodes, an upper semiconductor chip is placed above the lower semiconductor chip, ~~a wire connects~~ wires

semiconductor chip of said partially overlapped upper and lower semiconductor chips, and said second die pad ~~portion~~ supports said upper semiconductor chip.

12. (Amended) The semiconductor device according to claim 11, including adhesive layers respectively bonding said upper and lower semiconductor chips to said first and second die pads wherein a center of the thickness of said first die pad portion and a center of the thickness of said second die pad portion are spaced ~~vertically~~ from said reference plane in respective ~~directions~~ opposite ~~to each other~~ directions, each by a distance equal to the sum of ~~a~~ one-half ~~of~~ the thickness of said lead frame and ~~a~~ one-half ~~of~~ the thickness of ~~an~~ said adhesive ~~layer~~ layers bonding said upper and lower semiconductor chips to said first and second die pads.

13. (Amended) A method of manufacturing a semiconductor device comprising:

~~a lead frame stacking step of~~ stacking a first lead frame on a second lead frame, said first lead frame including a first lead portion and a first die pad ~~portion~~ extending in an L-shape from an end of said first lead portion along a periphery of a region where a lower semiconductor chip is arranged, said second lead frame including a second lead portion and a second die pad ~~portion~~ opposing said first die pad ~~portion~~, in plan view, and extending in an L-shape from an end of said second lead portion along a periphery of a region where an upper semiconductor chip is arranged, said first and second lead portions ~~opposing~~ being opposite each other, in plan view, with said upper and lower semiconductor chips therebetween;

~~a semiconductor chip bonding step of~~ bonding said lower semiconductor chip to said first die pad ~~portion~~ and bonding said upper semiconductor chip to said second die pad ~~portion~~;

~~a welding step of~~ welding together said first lead frame and said second lead frame ~~at their overlapping portion~~ where they overlap;

~~a wire bonding step of~~ connecting said upper and lower semiconductor chips to a terminal electrode ~~by~~ with a wire;

connect the upper and lower semiconductor chips to the terminal electrodes, and an encapsulating resin encapsulates the upper and lower semiconductor chips and ~~wire~~ wires. The encapsulating resin has its bottom surface coplanar with the bottom surface of the terminal electrodes.

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CLAIMS PENDING AFTER PRELIMINARY AMENDMENT

1. A semiconductor device having:

terminal electrodes located, in plan view, outside a region where semiconductor chips are located;

a lower semiconductor chip overlapping in height with said terminal electrodes;

an upper semiconductor chip located opposite said lower semiconductor chip;

wires connecting said upper and lower semiconductor chips to said terminal electrodes; and

an encapsulating resin encapsulating said upper and lower semiconductor chips and said wires, wherein said encapsulating resin and said terminal electrodes have respective bottom surfaces coplanar with each other.

2. The semiconductor device according to claim 1, including a die pad supporting said upper semiconductor chip and coplanar with said terminal electrodes, and wherein said lower semiconductor chip does not overlap, in plan view, said die pad.

3. The semiconductor device according to claim 1, wherein said lower semiconductor chip and said encapsulating resin have respective bottom surfaces coplanar

with each other and the bottom surface of said lower semiconductor chip is exposed and not covered by said encapsulating resin.

4. The semiconductor device according to claim 1, including a die pad supporting said upper semiconductor chip and not coplanar with said terminal electrodes, and wherein said lower semiconductor chip has a bottom surface encapsulated by said encapsulating resin.

5. The semiconductor device according to claim 1, wherein said semiconductor device is a QFN (Quad Flat Non-Lead) Package having said terminal electrodes surrounding said upper and lower semiconductor chips.

6. The semiconductor device according to claim 1, wherein said upper and lower semiconductor chips are respectively rectangular in shape, connection terminals of said upper and lower semiconductor chips are arranged along shorter sides of said upper and lower semiconductor chips, opposing each other, and said upper and lower semiconductor chips cross each other, in plan view.

7. The semiconductor device according to claim 1, wherein said terminal electrodes are leads located along two opposing sides of said semiconductor device with said upper and lower semiconductor chips therebetween.

8. A semiconductor device TSOP (Thin Small Outline) Package having:

upper and lower semiconductor chips arranged between a first lead portion and a second lead portion, respectively, on two opposing sides of said semiconductor device, in plan view;

a first die pad integrated with and not coplanar with said first lead portion and located on one side of a reference plane passing through a central position between a first surface and a second surface of said first and second lead portions; and

a second die pad integrated with and not coplanar with said second lead portion and located on a second side of the reference plane, wherein said lower semiconductor

chip is supported by said first die pad and said upper semiconductor chip is supported by said second die pad portion, said upper and lower semiconductor chips are partially overlapping and overlap in height with said first and second lead portions.

9. The semiconductor device according to claim 8, including:

a first lead frame connected to said first die pad and located, with said first lead portion, on the first side of said reference plane, and

a second lead frame connected to said first die pad and located, with said second lead portion, on the second side of said reference plane.

10. The semiconductor device according to claim 9, wherein

said first die pad portion is L-shaped and includes a first extension extending from an end of said first lead portion toward said second lead portion, and a first opposing portion continuing from said first extension and extending parallel to said first lead portion,

said second die pad portion is arranged, in plan view, opposite said first die pad , is L-shaped, and includes a second extension extending from an end of said second lead portion toward said first lead portion and a second opposing portion continuing from said second extension and extending parallel to said second lead portion,

said first extension and said first opposing portion have bottom surfaces supporting said lower semiconductor chip, and

said second extension and said second opposing portion have upper surfaces supporting said upper semiconductor chip.

11. The semiconductor device according to claim 8, wherein said first and second lead portions and said first and second die pads are integrated into a common lead frame, said reference plane passes centrally through the thickness of said lead frame, said first die pad supports said lower semiconductor chip of said partially overlapped upper and lower semiconductor chips, and said second die pad supports said upper semiconductor chip.

12. The semiconductor device according to claim 11, including adhesive layers respectively bonding said upper and lower semiconductor chips to said first and second die pads wherein a center of the thickness of said first die pad portion and a center of the thickness of said second die pad portion are spaced from said reference plane in respective opposite directions, each by a distance equal to the sum of one-half the thickness of said lead frame and one-half the thickness of said adhesive layers bonding said upper and lower semiconductor chips to said first and second die pads.

13. A method of manufacturing a semiconductor device comprising:

stacking a first lead frame on a second lead frame, said first lead frame including a first lead portion and a first die pad extending in an L-shape from an end of said first lead portion along a periphery of a region where a lower semiconductor chip is arranged, said second lead frame including a second lead portion and a second die pad opposing said first die pad, in plan view, and extending in an L-shape from an end of said second lead portion along a periphery of a region where an upper semiconductor chip is arranged, said first and second lead portions being opposite each other, in plan view, with said upper and lower semiconductor chips therebetween;

bonding said lower semiconductor chip to said first die pad and bonding said upper semiconductor chip to said second die pad;

welding together said first lead frame and said second lead frame ;

connecting said upper and lower semiconductor chips to a terminal electrode with a wire;

encapsulating in a resin a region inside of said first and second lead frames that have been welded; and

cutting off a portion, outside said resin, encapsulating said first and second lead portions and said upper and lower semiconductor chips.

14. The method of manufacturing a semiconductor device according to claim 13, including combining stacking of said first and second lead frames and bonding of said upper and lower semiconductor chips, and wherein sub steps in the lead frame stacking and sub steps in the semiconductor chip bonding are partially changed in their order.

12. The semiconductor device according to claim 11, including adhesive layers respectively bonding said upper and lower semiconductor chips to said first and second die pads wherein a center of the thickness of said first die pad portion and a center of the thickness of said second die pad portion are spaced from said reference plane in respective opposite directions, each by a distance equal to the sum of one-half the thickness of said lead frame and one-half the thickness of said adhesive layers bonding said upper and lower semiconductor chips to said first and second die pads.

13. A method of manufacturing a semiconductor device comprising:

stacking a first lead frame on a second lead frame, said first lead frame including a first lead portion and a first die pad extending in an L-shape from an end of said first lead portion along a periphery of a region where a lower semiconductor chip is arranged, said second lead frame including a second lead portion and a second die pad opposing said first die pad, in plan view, and extending in an L-shape from an end of said second lead portion along a periphery of a region where an upper semiconductor chip is arranged, said first and second lead portions being opposite each other, in plan view, with said upper and lower semiconductor chips therebetween;

bonding said lower semiconductor chip to said first die pad and bonding said upper semiconductor chip to said second die pad;

welding together said first lead frame and said second lead frame where they overlap;

connecting said upper and lower semiconductor chips to a terminal electrode with a wire;

encapsulating in a resin a region inside of said first and second lead frames that have been welded; and

cutting off a portion, outside said resin, encapsulating said first and second lead portions and said upper and lower semiconductor chips.

14. The method of manufacturing a semiconductor device according to claim 13, including combining stacking of said first and second lead frames and bonding of said

upper and lower semiconductor chips, and wherein sub steps in the lead frame stacking and sub steps in the semiconductor chip bonding are partially changed in their order.

15. The method of manufacturing a semiconductor device according to claim 13, including combining stacking of said first and second lead frames and bonding of said upper and lower semiconductor chips, and wherein bonding said upper and lower semiconductor chips includes arranging a die bonding material for bonding said upper and lower semiconductor chips to said first and second die pad.

PATENT
Attorney Docket No. 401263/FUKAMI

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

ABE et al.

Application No.: Unknown

Art Unit: Unkn

Examiner: Unknown

Filed: June 28, 2001

For: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

REQUEST FOR APPROVAL OF CHANGES TO THE DRAWINGS

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

The Examiner is requested to approve the changes to Figures 9-21 and 29-35, as shown in red on the attached sheets of drawings.

Respectfully submitted,

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Date: June 28, 2001
JAW:ves

FIG. 9

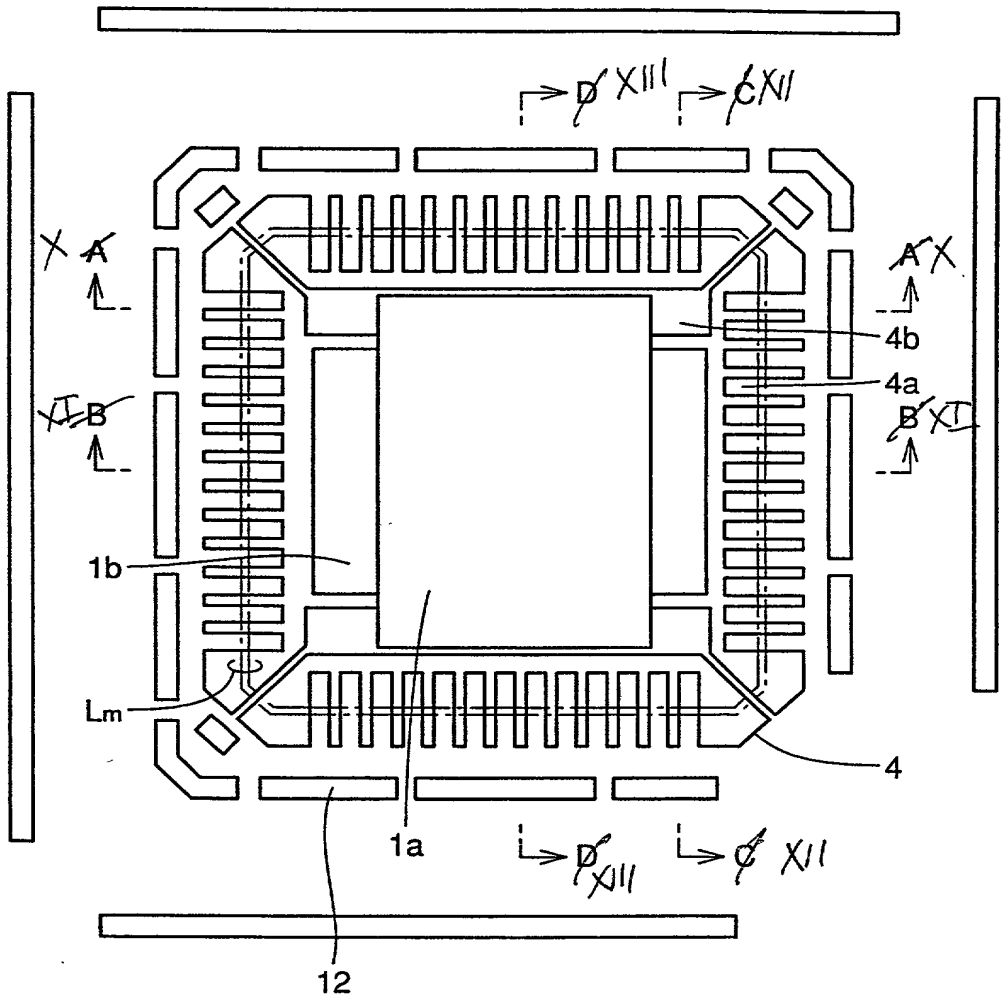

FIG. 10

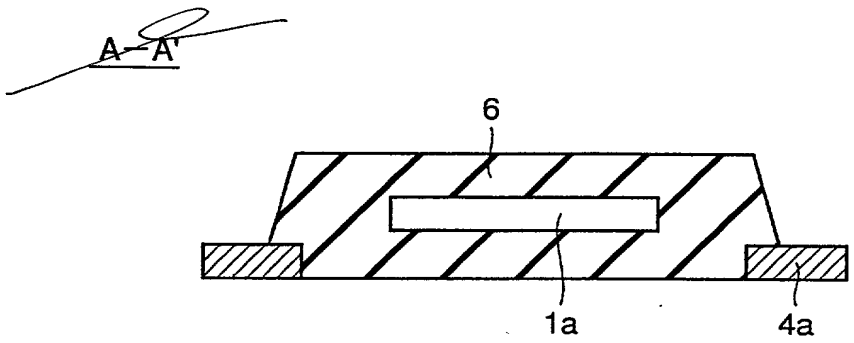

FIG. 11

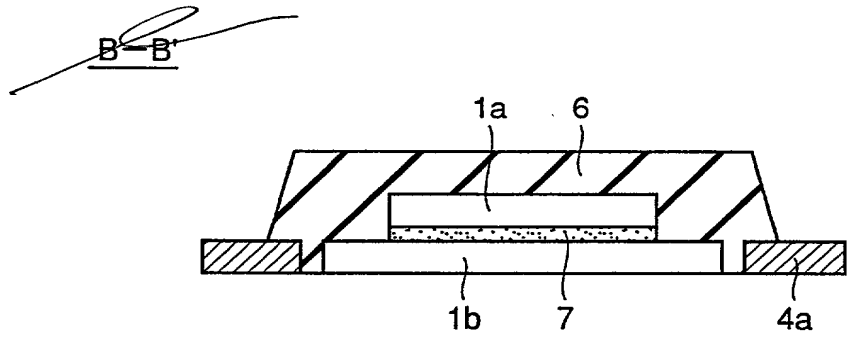

FIG. 12

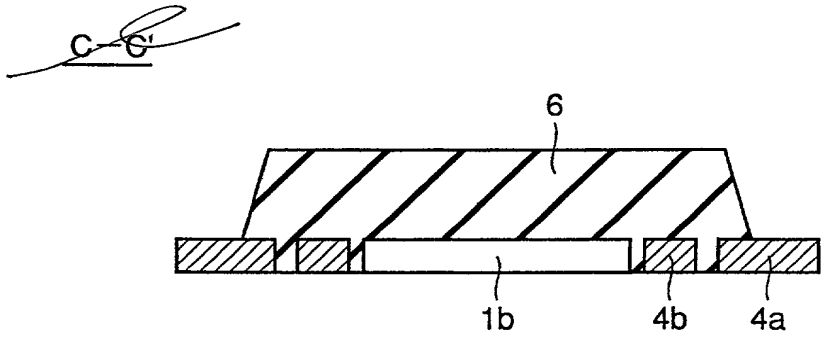

FIG. 13

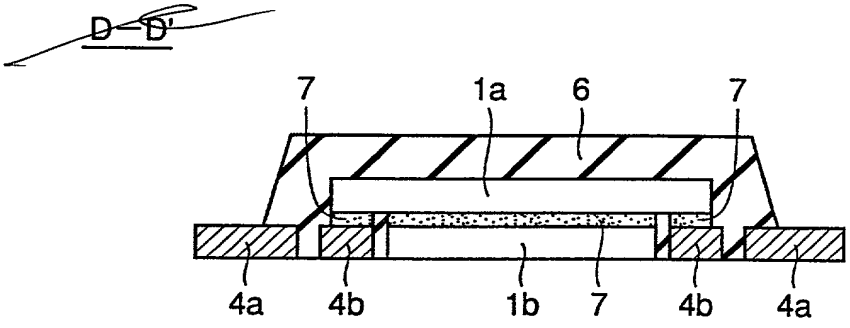

FIG. 14

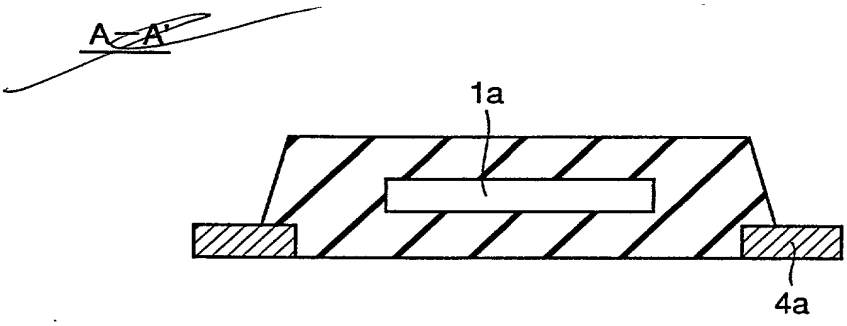

FIG. 15

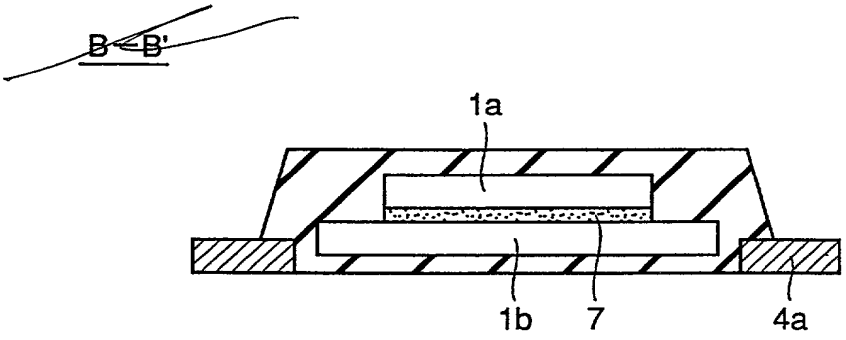

FIG. 16

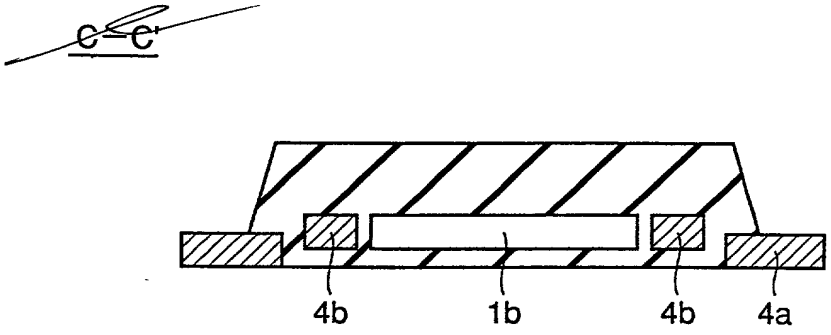

FIG. 17

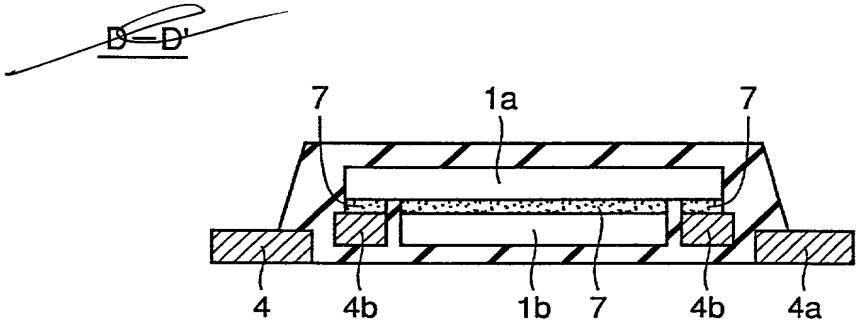

FIG. 18

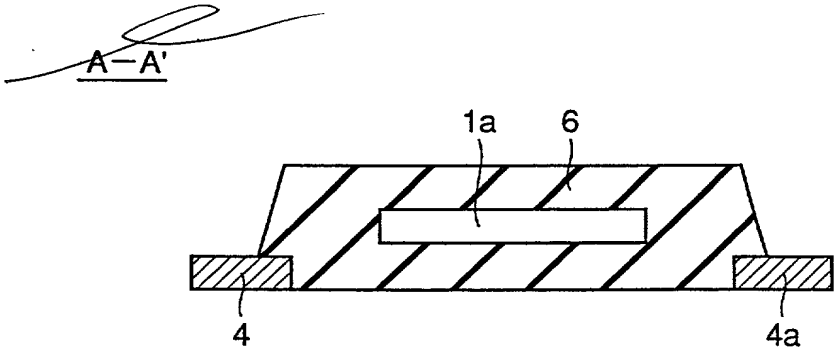

FIG. 19

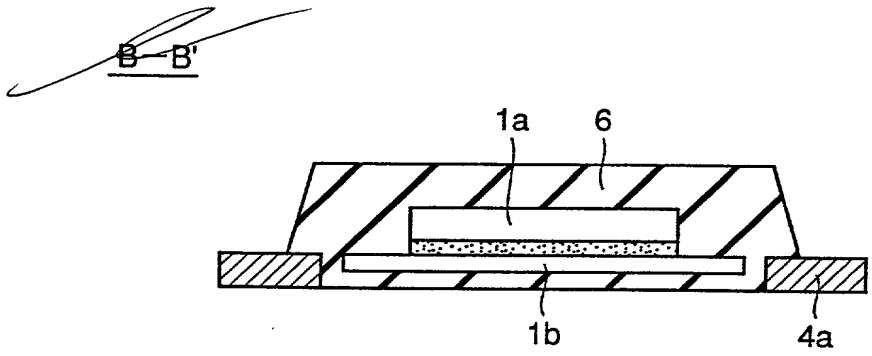

FIG. 20

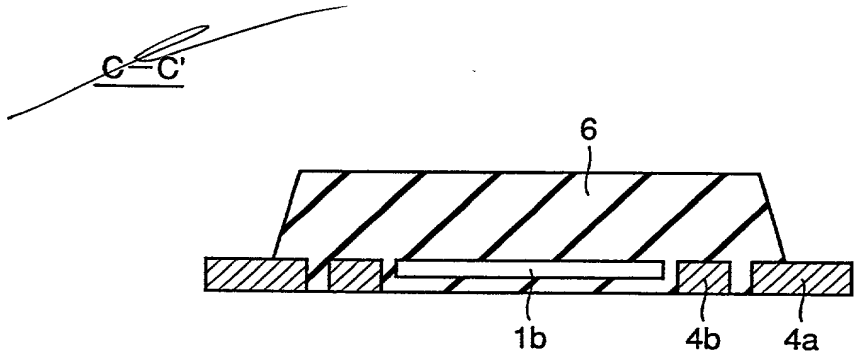

FIG. 21

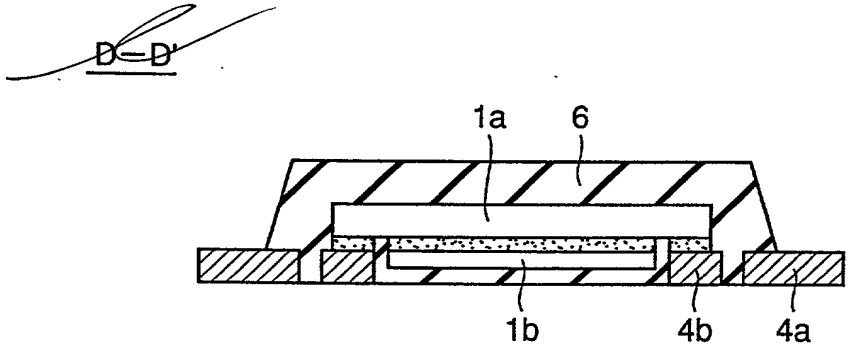

FIG. 29

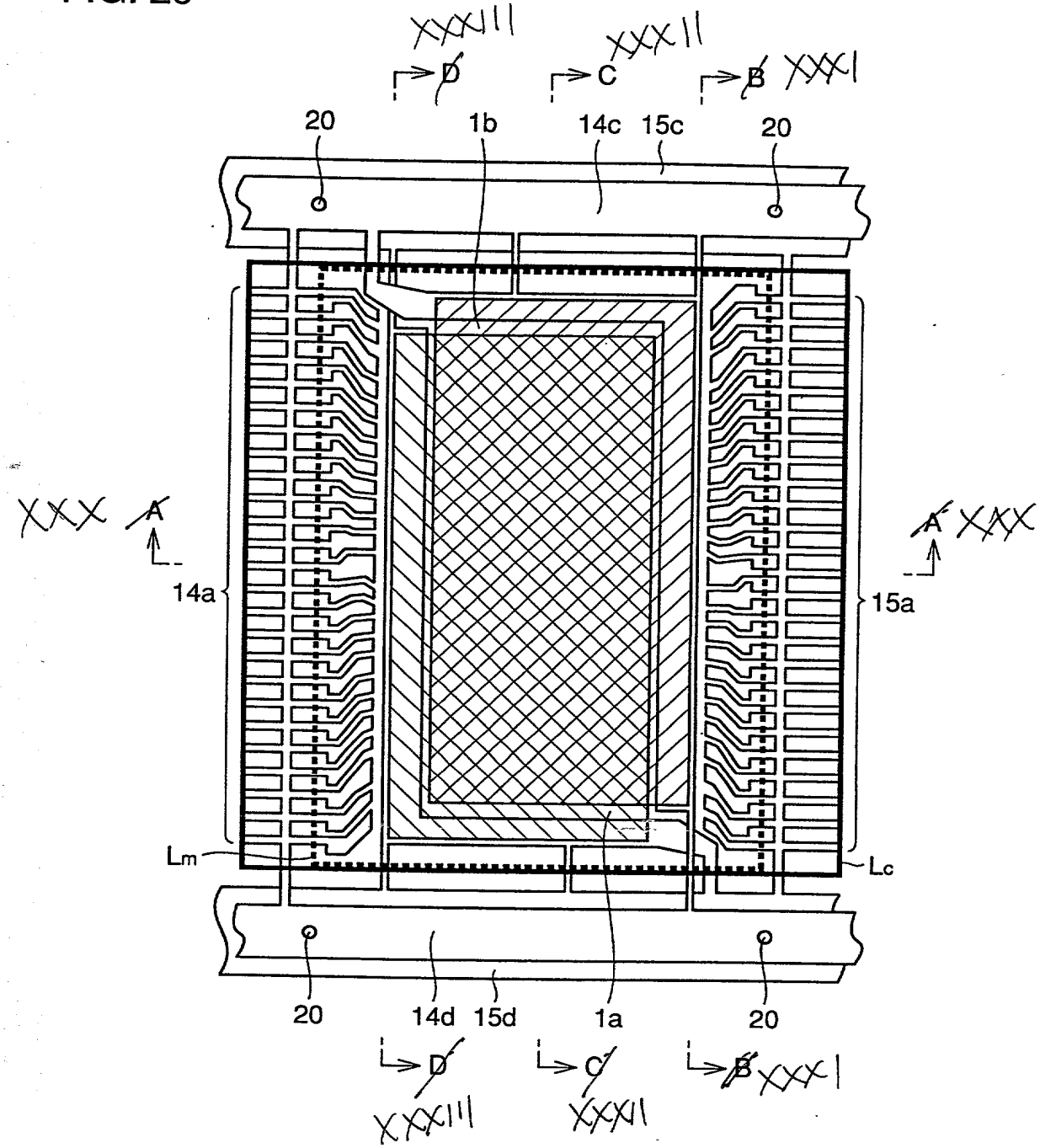

FIG. 30

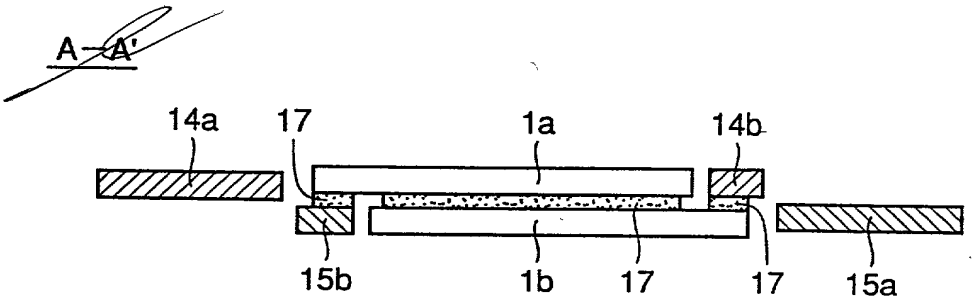

FIG. 31

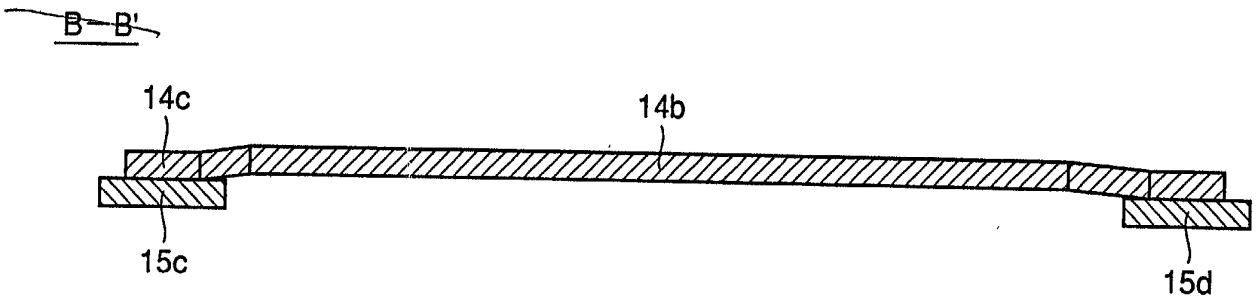

FIG. 32

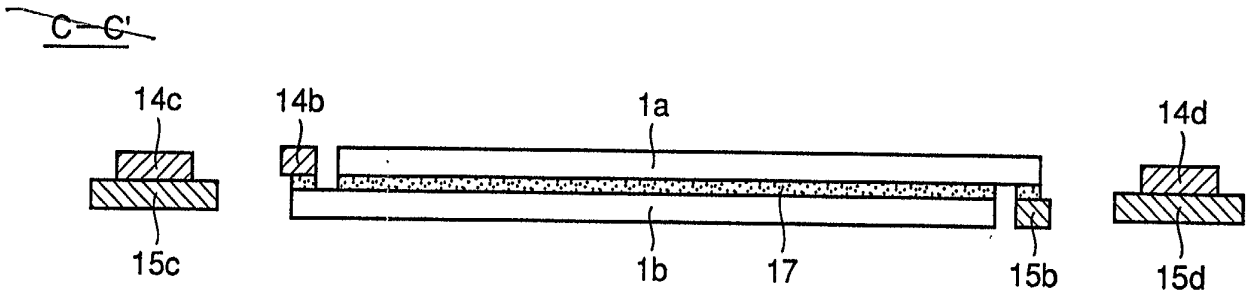

FIG. 33

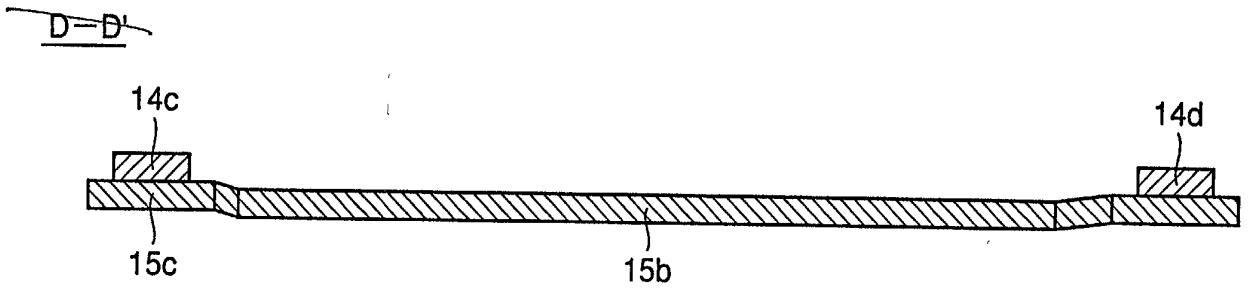

FIG. 34

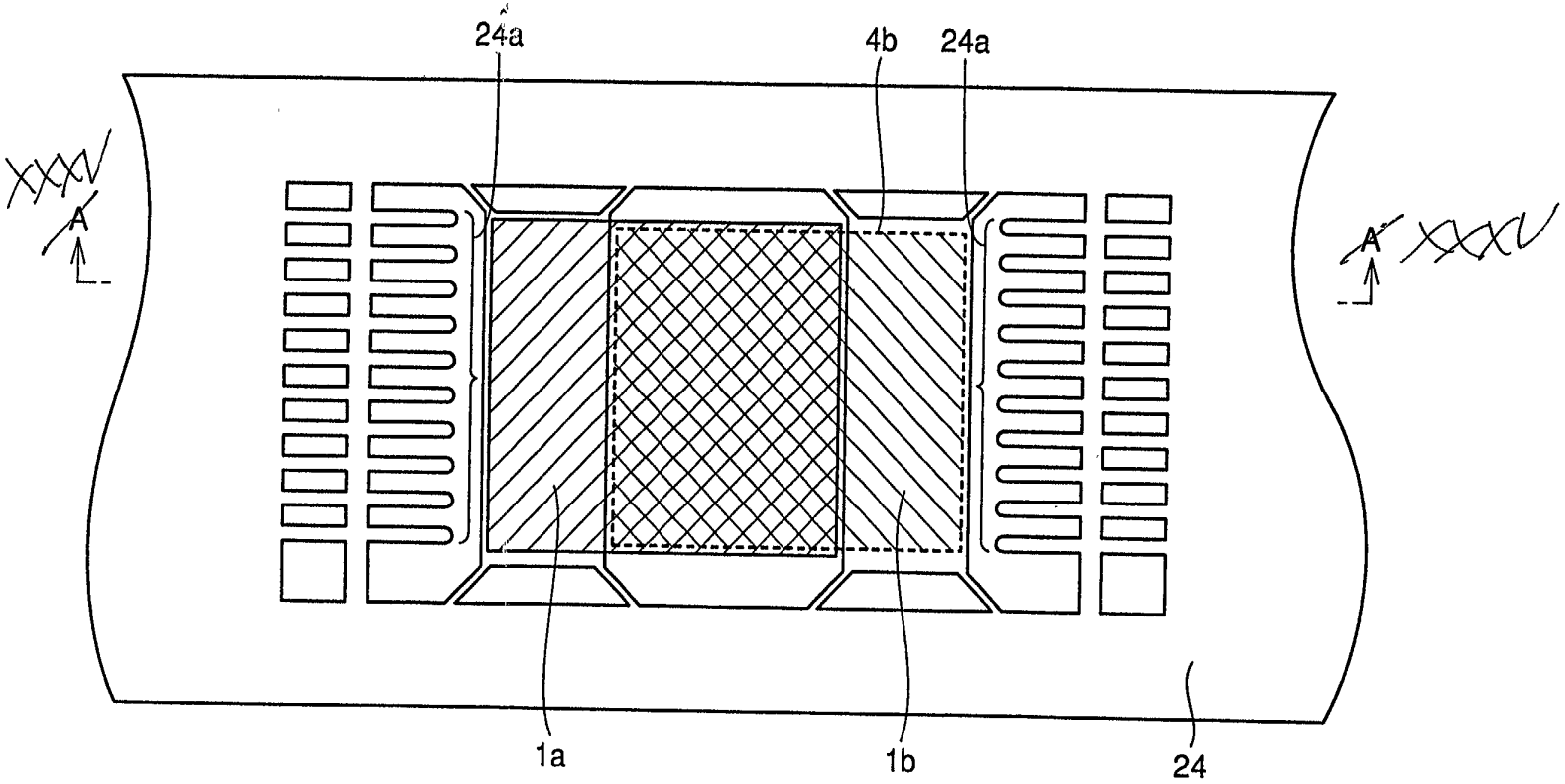

FIG. 35

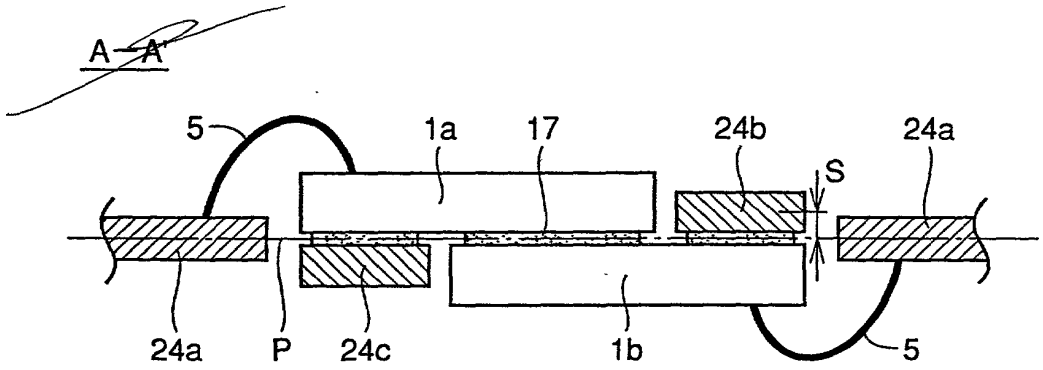

FIG. 36 PRIOR ART

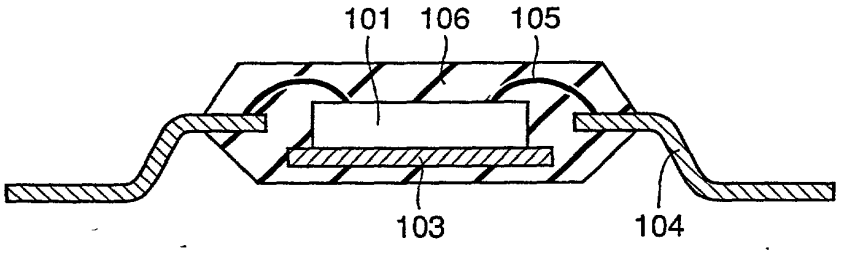

FIG. 37 PRIOR ART